Amendments to the Specification:

Please replace the Abstract paragraph at page 28 with the following rewritten Abstract:

Semiconductor packages are disclosed. One semiconductor package includes a semiconductor die with an active surface, an opposite inactive surface, and four peripheral side surfaces. A substrate of the semiconductor package is coupled to one side surface of the semiconductor die. Bond pads of the active surface are coupled to a substrate first surface that is coplanar with the active surface. External interconnects, e.g., solder balls, are formed on a second substrate surface that is perpendicular to the active surface. An insulating layer, e.g., ~~and~~ an encapsulant, together covers the active surface and the substrate first surface. An alternative semiconductor package includes two substrates, each attached to a respective one of two opposed side surfaces of the semiconductor die. The remaining two side surfaces of the semiconductor die are exposed. The external interconnects are formed on a third substrate surface that is coplanar with the inactive surface of the semiconductor die.

Please replace paragraph **[0047]** with the following rewritten paragraph:

The active surface 211 of the semiconductor die 210, the bond pads 215, the conductive wires 240, the peripheral surface 220a of the adhesive layers 220, the third surface ~~232~~ 231 of the substrates 230, and the bond fingers 234 of semiconductor package 200 are entirely covered by an electrically insulative encapsulant 250, which may be a hardened epoxy mold compound or a hardened liquid encapsulant. The encapsulant 250 includes a planar exposed first surface 251, and a planar unexposed second surface 252 that is opposite the first surface 251. The second surface 252 is formed on and bonded to the active surface 211, the peripheral surface 220a of each of the adhesive layers 220,

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and the third surface 231 of each substrate 230, all of which surfaces are coplanar. The encapsulant 250 also includes four rectangular planar peripheral surfaces that are between and perpendicular to the first and second surfaces 251, 252. Two of those four peripheral side surfaces of encapsulant 250, i.e., third surface 253 and parallel opposite fourth surface 254, are shown. The third surface 253 and the fourth surface 254 of the encapsulant 250 ~~is~~ are flush with the second surfaces 233b of the substrates 230~~, and the fourth surface 254 of the encapsulant 250 is flush with the side surface 214 of the semiconductor die 210~~. Accordingly, the inactive surface 212 and two of the four peripheral side surfaces (see FIG. 1A) of the semiconductor die 210 (i.e., the two others besides side surfaces 213, 214) are exposed to the outside environment, which provides semiconductor package 200 with excellent heat radiation and a near-chip size.

Please replace paragraph **[0052]** with the following rewritten paragraph:

Referring to FIGS. 3A-3C, the semiconductor package 300 includes a semiconductor die 310, a layer of an insulative adhesive 320 bonded on a peripheral side 313 of the semiconductor die 310, a substrate 330 bonded to the adhesive 320 opposite semiconductor die 310, two insulative layers 340, 350 that successively overlie the active surface ~~313~~ 311 of semiconductor die 310 and that include conductive circuit patterns that electrically couple the semiconductor die 310 to the substrate 330, and a plurality of solder balls 360 fused to a peripheral surface 333b of the substrate 330.

Please replace paragraph **[0053]** with the following rewritten paragraph:

The semiconductor die 310 has the form of a rectangular prism, and includes an active surface 311 and an inactive

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surface 312 opposed to the active surface 311. The semiconductor die 310 further includes four planar rectangular peripheral side surfaces that are between and perpendicular to the active and inactive surfaces 311 and 312. Two of those four peripheral side surfaces, i.e., a third surface ~~331~~ 313 and an opposite parallel fourth surface ~~334~~ 314, are shown. A plurality of bond pads 315 are formed at the active surface 311 of semiconductor die 310. In this example, the bond pads 315 are arranged in a single row that is adjacent to the side surface 313. There are no corresponding bond pads 315 along side surface 314. The thickness of the semiconductor die 310, which is not back-grinded or otherwise thinned, is approximately 29 mils between the active and inactive surfaces 311, 312.

Please replace paragraph **[0055]** with the following rewritten paragraph:

The substrate 330 is bonded to the adhesive 320. The substrate 330 has the form of a rectangular prism, and includes a rectangular major first surface 333a that faces side surface 313 of semiconductor die 310 and is coupled thereto by adhesive 320, a rectangular major second surface 333b opposed to the first surface 333a, and four rectangular planar peripheral surfaces that are perpendicular to and between the first and second surfaces 333a, 333b. Two of the four peripheral side surfaces, i.e., a third surface ~~333~~ 331 and an opposite parallel fourth surface 332, are shown. First and second surfaces 333a, 333b of substrate 330 have the same, or approximately the same, area as side surface 313 of semiconductor die 310. First surface 333a is entirely covered by the adhesive layer 320. The third surface 331 of the substrate 330 is flush with (i.e., coplanar with) the active surface 311 of the semiconductor die 310, and the fourth surface 332 of the substrate 330 is flush with the inactive

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surface 312 of the semiconductor die 310. The thickness of substrate 330 between first and second surfaces 333a, 333b is much less than the thickness of semiconductor die 310 between side surfaces 313, 314. Accordingly, the whole size of the semiconductor package 300 is close to that of the semiconductor die 310 alone.

Please replace paragraph **[0057]** with the following rewritten paragraph:

The active surface 311 of the semiconductor die 310, the bond pads 315, the planar surface 320a of adhesive layer 320, the third surface ~~333~~ 331 of the substrate 330, and the bond fingers 334 are entirely covered by a protective electrically-interconnective structure that, in this example, is formed by successive layers 340, 350 of an electrically insulative material (e.g., polyimide, ceramic, epoxy resin) through which and/or on which electrically conductive circuit patterns 341, 342, and 351 extend.

Please replace paragraph **[0060]** with the following rewritten paragraph:

The first and second insulating layers 340, 350 are rectangular in area, and successively cover the active surface 311 of semiconductor die 310, the adhesive layer surface 320a, and the third surface 331 of substrate 330, all of which surfaces are coplanar. The first and second insulating layers include rectangular major peripheral surfaces 340a, 350a, respectively. The four peripheral side surfaces of first and second insulating layers 340, 350 that extend perpendicularly between major surface 350a of second layer 350 and active surface 311, of which two parallel opposed side surfaces 352, 354 are shown, are flush with, i.e., coplanar with, the corresponding peripheral sides of semiconductor die 310 or substrate 330, e.g., side surface ~~352~~ 354 is flush with side

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surface 314 of semiconductor die 310 and side surface ~~354~~ 352 is flush with second surface 333b of substrate 330.

Please replace paragraph **[0065]** with the following rewritten paragraph:

In the mounting of FIG. 3C, the semiconductor package 300 is mounted so that side surface 313 of semiconductor die 310, second surface 333b of substrate 330, and side surface 352 of first and second insulating layers 340, 350 are parallel to and face the mounting surface 370a of external device 370. Side surface 314 of semiconductor die 310 and side surface 354 of ~~encapsulant 350~~ of first and second insulating layers 340, 350 are parallel to, but face away from, the mounting surface 370a of external device 370. The active and inactive surfaces 311, 312 of semiconductor die 310, the third and fourth surfaces 331, 332 of substrate 330, and the long dimension of first and second insulating layers 340, 350 are perpendicular to the mounting surface 370a of external device 330. Accordingly, the area of mounting surface 370a occupied by semiconductor package 300 is very small, which allows for a high mounting density. Further, the zigzag pattern of the solder balls 360 allows for the joints between the solder balls 360 and the mounting surface 370a to be in a zigzag pattern, which provides for a high strength connection between the semiconductor package 300 and the external device 370.

Please replace paragraph **[0073]** with the following rewritten paragraph:

Each of the two substrates 430 is bonded to a respective one of the adhesive layers 420. The substrate 430 has the form of a rectangular prism, and includes a rectangular major first surface 433a that faces, is parallel to, and coextensive with the respective adjacent side surface 413, 414 of semiconductor die 410 and is coupled thereto by the adhesive 420, a

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rectangular major second surface 433b parallel to and opposed to the first surface 433a, and four planar peripheral surfaces perpendicular to and between the first and second surfaces 433a, 433b. Two of the four peripheral surfaces, a third surface 431 and an opposite parallel fourth surface 432, are shown. The third surface 431 of the substrate 430 is flush with (i.e., coplanar with) the active surface 411 of the semiconductor die 410, and the opposite fourth surface ~~434~~ 432 of the substrate 430 is flush with the inactive surface ~~414~~ 412 of the semiconductor die 410. The thickness of substrate 430 between first and second surfaces 433a, 433b is much less than the thickness of semiconductor die 410 between side surfaces 413, 414. Accordingly, the whole size of the semiconductor package 400 is close to that of the semiconductor die 410 alone.

Please replace paragraph **[0074]** with the following rewritten paragraph:

Each substrate 430 includes an electrically insulative core, which may be formed of one or more layers of any suitable insulative material, such as polyimide, FR4, epoxy resin, ceramic, and the like. The substrate 430 further includes a plurality of electrically conductive circuit patterns at the surface of, and within, the core insulative layer of substrate 430, including a plurality of bond fingers 434 at the third surface 431 and a plurality of ball lands 435 at the opposite fourth surface ~~434~~ 432 thereof. Here, the ball lands 435 are formed in a single row on each of the substrates 430. A plurality of electrically conductive vias 436 extend straight through the insulative core of substrate 430 between the third surface 431 and the fourth surface ~~434~~ 432. Each of the bond fingers 434 of each substrate 430 is electrically coupled to a respective one of the to the ball lands 435 by a respective one of the conductive vias 436.

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Please replace paragraph **[0077]** with the following rewritten paragraph:

The second insulating layer 450 contacts, is bonded to, and covers the first insulating layer 440 opposite the active surface 411. The second insulating layer 450 includes a plurality of conductive circuit patterns 451 that extend through second insulating layer 450 in a direction parallel to the active surface 411 and to the long dimension of layers ~~340, 350~~ 440, 450, and perpendicular to conductive circuit patterns 441, 442. Each conductive pattern 451 extends between and electrically couples one of the conductive circuit patterns 441 and one of the conductive circuit patterns 442. Accordingly, the bond pads 415 of the semiconductor die 410 and the bond fingers 434 of the substrate 430 are electrically connected to each other by means of the first conductive circuit patterns 441 and 442 and the intervening second conductive circuit patterns 451. A surface 451a of each of the conductive circuit patterns 451 is exposed at the outer exposed surface 450a of the second insulating layer 450.

Please replace paragraph **[0078]** with the following rewritten paragraph:

The major surfaces 440a, 450a of the first and second insulating layers 440, 450, respectively, are rectangular in area, and are parallel to the active surface 411 of semiconductor die 410 and third surface ~~441~~ 431 of substrate ~~440~~ 430. The four peripheral side surfaces of the first and second insulating layers 440, 450, of which two opposed parallel side surfaces 452, ~~454~~ 453 are shown, are flush with, i.e., coplanar with the corresponding peripheral surfaces of the semiconductor die 410 or substrate 430, e.g., side surface 452 and side surface 453 are ~~is flush with side surface 414 of~~

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~~semiconductor die 410 and side surface 454 is~~ flush with second surfaces 433b of substrates 430.

Please replace paragraph **[0082]** with the following rewritten paragraph:

In the mounting of FIG. 4C, the semiconductor package 400 is mounted so that the inactive surface ~~414~~ 412 of semiconductor die 410, and the second surface 432 of the substrates 430 face and are parallel to the mounting surface 470a of external device 470. Accordingly, the area of mounting surface 470a occupied by semiconductor package 400 is small, which allows for a high mounting density.

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